IN THE CLAIMS:

Please amend claims 1-40 and please cancel claims 41-45 as provided below.

1. (Currently amended) An electronic transmitter device ~~having~~ comprising a puncturing device, wherein the puncturing device comprises:

[[-]] ~~has~~ a first and a second data output,

[[-]] and wherein the puncturing device is configured in such a way that it distributes ~~its~~ an output data stream ~~essentially~~ substantially uniformly in parallel between ~~its said two~~ the first and second data outputs,

[[-]] and wherein the puncturing device is further configured to provide[[s]] empty locations in ~~it's~~ the output data stream so that ~~the~~ a number of bits of ~~the~~ an input data stream corresponds, including the empty locations, to ~~the~~ a number of bits of the output data stream, and

[[-]] wherein the puncturing device is still further configured to output[[s]] in addition to ~~it's~~ the parallel output data stream, a signal which indicates ~~to~~ a position of the puncturing device empty locations in the parallel output data stream.

2. (Currently amended) An electronic transmitter device, comprising ~~having~~ an interleaver ~~(2), characterized in that the interleaver (2) has~~ comprising two data inputs, and ~~is~~ configured in such a way that ~~it can~~ the interleaver processes data streams ~~coming in~~ received in parallel at both data inputs.

3. (Currently amended) The electronic transmitter device as claimed in claim 2, ~~characterized in that~~ wherein the interleaver ~~(2) is~~ comprises a block interleaver which has parallel data inputs.

4. (Currently amended) The electronic transmitter device as claimed in claim 1, ~~characterized in that it has~~ further comprising an interleaver ~~(2) which is~~ arranged

downstream of the puncturing device in ~~the~~ a direction of the data stream, and ~~which~~comprising:

[[-]] ~~has~~ a first data input which is directly or indirectly electrically connected to the first data output of the puncturing device, and

[[-]] a second data input which is directly or indirectly electrically connected to the second data output of the puncturing device.

5. (Currently amended) The electronic transmitter device as claimed in ~~one of~~ claim[[s]] 2 ~~to 4~~, ~~characterized in that~~ wherein the interleaver ~~(2) is~~ comprises an n x m interleaver, n and m being natural numbers.

6. (Currently amended) The electronic transmitter device as claimed in ~~one of~~ claim[[s]] 2 ~~to 5~~, ~~characterized in that~~ wherein the interleaver ~~(2) has~~ comprises a first shift register which is directly or indirectly electrically connected to its first data input, and a second shift register which is directly or indirectly electrically connected to its second data input.

7. (Currently amended) The electronic transmitter device as claimed in claim 6, ~~which is referred back to claim 5, characterized in that~~ wherein both shift registers are 8-bit shift registers.

8. (Currently amended) The electronic transmitter device as claimed in claim 6 ~~or 7~~, ~~characterized in that~~ wherein the interleaver ~~(2) has~~ comprises a matrix register.

9. (Currently amended) The electronic transmitter device as claimed in claim 8, ~~characterized in that~~ wherein the matrix register ~~is~~ comprises a 16 x 18 matrix register.

10. (Currently amended) The electronic transmitter device as claimed in claim 8 ~~or 9~~, ~~characterized in that~~ wherein in each case two bits are written in parallel into the matrix register from the two shift registers.

11. (Currently amended) The electronic transmitter device as claimed in claim 8 ~~or 9~~, ~~characterized in that~~ wherein after the two shift registers have been completely filled by inputs via the corresponding data inputs of the interleaver ~~(2)~~, their bits are input together as a bit column into the matrix register, interleaved in the manner of a comb, and in this way ~~they~~ the bits gradually fill up a plurality of, or all of, the columns of the matrix register.

12. (Currently amended) The electronic transmitter device as claimed in ~~one of~~ claim[[s]] 2 ~~to 5~~, ~~characterized in that~~ wherein the interleaver ~~(2) has~~ comprises an RAM and is designed in such a way that the bit pairs which pass into the interleaver ~~(2)~~ are written directly to predetermined RAM addresses.

13. (Currently amended) The electronic transmitter device as claimed in claim 4, ~~characterized in that~~
[[-]] wherein the interleaver ~~(2)~~ is configured in such a way that, using the ~~said~~ indication signal ~~(data_valid)~~ which is additionally transmitted by the puncturing device, ~~it~~ the interleaver detects the empty locations in the parallel input data stream coming from the puncturing device, and does not include them in the further data processing.

14. (Currently amended) The electronic transmitter device as claimed in claim 1, ~~characterized in that~~ wherein the puncturing device ~~is composed of precisely~~ comprises one puncturing element ~~(P2)~~.

15. (Currently amended) The electronic transmitter device as claimed in claim 1, ~~characterized in that~~ wherein the puncturing device ~~has~~ comprises a first puncturing

element ~~(P1)~~ and a second puncturing element ~~(P2)~~ which is arranged downstream of the first puncturing element ~~(P1)~~ in the direction of the data stream.

16. (Currently amended) The electronic transmitter device as claimed in claim 15, ~~characterized in that~~ wherein:

[[-]] the first puncturing element ~~(P1) has~~ comprises a first and a second data output and is configured in such a way that it distributes its output data stream ~~essentially~~ substantially uniformly between its two data outputs, and

[[-]] the second puncturing element ~~(P2) has~~ comprises a first and a second data input, the first data input of the second puncturing element ~~(P2)~~ being directly or indirectly electrically connected to the first data output of the first puncturing element ~~(P1)~~, and the second data input of the second puncturing element ~~(P2)~~ being directly or indirectly electrically connected to the first data output of the first puncturing element ~~(P1)~~.

17. (Currently amended) The electronic transmitter device as claimed in claim 16, ~~characterized in that~~wherein:

[[-]] the first puncturing element ~~(P1)~~ is configured in such a way that, in addition to its parallel output data stream, ~~it~~ the first puncturing element transmits to the second puncturing element ~~(P2) a~~ the indication signal ~~(data_valid)~~ which informs the second puncturing element ~~(P2)~~ about empty locations in the parallel output data stream of the first puncturing element ~~(P1)~~, and

[[-]] the second puncturing element ~~(P2)~~ is configured in such a way that, using the ~~said~~ indication signal ~~(data_valid)~~ which is additionally transmitted by the first puncturing element ~~(P1)~~, ~~it~~ the second puncturing element detects the empty locations in the parallel input data stream coming from the first puncturing element ~~(P1)~~, and does not include them in the further data processing.

18. (Currently amended) The electronic transmitter device as claimed in claim 16 ~~or claim 17~~, ~~characterized in that~~ wherein the first puncturing element ~~(P1) has~~ comprises a first data input ~~(IN_X)~~ and a second data input ~~(IN_Y)~~, and is configured in such a way that

[[-]] a 1-step delay register ~~(D)~~ is connected between the first data input ~~(IN_X)~~ and the first data output ~~(Out_X)~~,

[[-]] the second data input ~~(IN_Y)~~ is electrically connected to a first input of a multiplexer ~~(MUX)~~ via a 1-step delay register ~~(D)~~, and in parallel with this ~~it~~ the second data input is directly electrically connected to a second input of a multiplexer ~~(MUX)~~, and

[[-]] the multiplexer ~~(MUX)~~ has an output which is electrically connected to the second data output ~~(Out_Y)~~ of the first puncturing element ~~(P1)~~ via a further 1-step delay register ~~(D)~~.

19. (Currently amended) The electronic transmitter device as claimed in ~~one of~~ claim[[s]] 15 ~~to 18~~, ~~characterized in that~~ wherein the second puncturing element ~~(P2) has~~ comprises two data outputs.

20. (Currently amended) The electronic transmitter device as claimed in claim 19, ~~characterized in that~~ wherein the two data outputs of the second puncturing element ~~(P2)~~ are simultaneously the two data outputs of the puncturing device.

21. (Currently amended) The electronic transmitter device as claimed in claim 19 ~~or claim 20~~, ~~characterized in that~~wherein:

[[-]] the second puncturing element ~~(P2) has~~ comprises three multiplexers ~~(MUX)~~ which each have two inputs and one output,

[[-]] the first data input ~~(IN_X)~~ of the second puncturing element ~~(P2)~~ is directly electrically connected both to the first input of the first multiplexer of the second

puncturing element ~~(P2)~~ and to the first input of the second multiplexer of the second puncturing element ~~(P2)~~,

[[-]] the second data input ~~(IN_Y)~~ of the second puncturing element ~~(P2)~~ is directly electrically connected both to the second input of the first multiplexer of the second puncturing element ~~(P2)~~ and to the second input of the second multiplexer of the second puncturing element ~~(P2)~~,

[[-]] the output of the first multiplexer of the second puncturing element ~~(P2)~~ is directly electrically connected to the first input of the third multiplexer of the second puncturing element ~~(P2)~~,

[[-]] the output of the first multiplexer of the second puncturing element ~~(P2)~~ is electrically connected via a 1-step delay register ~~(D)~~ to the second input of the third multiplexer of the second puncturing element ~~(P2)~~,

[[-]] the output of the third multiplexer of the second puncturing element ~~(P2)~~ is electrically connected via a 1-step delay register ~~(D)~~ to the first data output ~~(Out_X)~~ of the second puncturing element ~~(P2)~~, and

[[-]] the output of the second multiplexer of the second puncturing element ~~(P2)~~ is electrically connected via a further 1-step delay register ~~(D)~~ to the second data output ~~(Out_Y)~~ of the second puncturing element ~~(P2)~~.

22. (Currently amended) An electronic receiver device ~~having~~ comprising a de-interleaver ~~(3)~~ which ~~has~~ comprises:

a first data output, and ~~characterized in that the de-interleaver (3)~~ ~~has~~ a second data output, ~~and~~

[[-]] wherein the de-interleaver is configured in such a way that it distributes its output data stream ~~essentially~~ substantially uniformly in parallel between ~~its said two~~ the first and second data outputs.

23. (Currently amended) The electronic receiver device as claimed in claim 22, ~~characterized in that~~ wherein the de-interleaver ~~(3) is~~ comprises an n x m de-interleaver, n and m being natural numbers.

24. (Currently amended) The electronic receiver device as claimed in claim 22 ~~or claim 23~~, ~~characterized in that~~ wherein the de-interleaver ~~(3) has~~ comprises a matrix register.

25. (Currently amended) The electronic receiver device as claimed in claim 24, ~~characterized in that~~ wherein the matrix register ~~is~~ comprises a 16 x (18 x N) matrix register, N being the word length of the soft bits.

26. (Currently amended) The electronic receiver device as claimed in claim 24 ~~or 25~~, ~~characterized in that~~ wherein the de-interleaver ~~(3)~~ is configured in such a way that in each case two soft bits are read out in parallel from the matrix register.

27. (Currently amended) The electronic receiver device as claimed in ~~one of~~ claim[[s]] 23 ~~to 26~~, ~~characterized in that~~ wherein the de-interleaver ~~(3) has~~ comprises a first shift register which is directly or indirectly electrically connected to its first data output, and a second shift register which is directly or indirectly electrically connected to its second data output, the two said shift registers being configured as soft bit shift registers.

28. (Currently amended) The electronic receiver device as claimed in claim 27, ~~which is referred back to claim 23, characterized in that~~ wherein both shift registers are soft bit shift registers.

29. (Currently amended) The electronic receiver device as claimed in claim 27, ~~or 28, characterized in that~~ wherein the de-interleaver ~~(3)~~ is configured in such a

way that, when the data is output from the n x m structure or from the matrix register, at first a column is output interleaved in ~~the manner of a comb, i.e.~~ a manner where the column is output to the two shift registers in such a way that two adjacent soft bits are respectively fed to a different shift register, and then both shift registers are read out simultaneously, and after the reading out of the two shift registers further data columns are successively output to the two shift registers from the n x m structure or from the matrix register in the same way as with the first column which is output.

30. (Currently amended) The electronic receiver device as claimed in claim 22, ~~characterized in that~~ wherein the de-interleaver ~~(3) has~~ comprises an RAM and is configured in such a way that when data is output the bit pairs from the RAM are fed directly to the two data outputs of the de-interleaver ~~(3)~~.

31. (Currently amended) An electronic receiver device, comprising: ~~having~~

[[-]] a de-interleaver; ~~(3)~~ and

[[-]] a depuncturing device which is arranged downstream of the de-interleaver ~~(3)~~ in the direction of the data stream, the de-interleaver comprising: ~~(3)~~

[[-]] ~~having~~ a first and a second data output,

[[-]] the de-interleaver being configured in such a way that it distributes its output data stream ~~essentially~~ substantially uniformly in parallel between ~~its said two~~ the first and second data outputs,

[[-]] and wherein the de-interleaver provides empty locations in its output data stream so that ~~the~~ a number of bits of the output data stream of the de-interleaver ~~(3)~~ corresponds, including the empty locations, to ~~the~~ a number of bits of the output data stream of the depuncturing device, and

[[-]] further wherein the de-interleaver transmits, in addition to its parallel output data stream, to the depuncturing device an indication signal ~~(data_valid)~~ which informs the depuncturing device about empty locations in the parallel output data stream of the de-interleaver ~~(3)~~.

32. (Currently amended) The electronic receiver device as claimed in claim 31, ~~characterized in that~~ wherein the depuncturing device which is arranged downstream of the de-interleaver ~~(3)~~ in the direction of the data stream ~~has~~ comprises two data inputs, the first data input of the depuncturing device being directly or indirectly electrically connected to the first data output of the de-interleaver ~~(3)~~, and the second data input of the depuncturing device being directly or indirectly electrically connected to the second data output of the de-interleaver ~~(3)~~.

33. (Currently amended) The electronic receiver device as claimed in claim 32, ~~characterized in that~~ wherein

[[-]] the depuncturing device is configured in such a way that, using the ~~said~~ indication signal ~~(data_valid)~~ which is additionally transmitted by the de-interleaver ~~(3)~~, ~~it~~ the depuncturing device detects the empty locations in the parallel input data stream coming from the de-interleaver ~~(3)~~ and fills ~~them~~ the empty locations with soft zeros during the further data processing.

34. (Currently amended) An electronic receiver device ~~having~~ comprising a depuncturing device, the depuncturing device ~~having~~ comprising two data inputs and being configured in such a way that ~~it can~~ the depuncturing device processes data streams ~~coming in~~ received in parallel at both data inputs, and ~~has~~ comprises a first depuncturing element ~~(P2')~~ and a second depuncturing element ~~(P1')~~ which is arranged downstream of the first depuncturing element ~~(P2')~~ in the direction of the data stream, wherein

[[-]] the first depuncturing element ~~(P2')~~ providing empty locations in its output data stream so that ~~the~~ a number of bits of the output data stream of the first depuncturing element ~~(P2')~~ corresponds, including the empty locations, to ~~the~~ a number of bits of the output data stream of the second depuncturing element ~~(P1')~~, and wherein

[[-]] the first depuncturing element ~~(P2')~~ is configured in such a way that, in addition to its parallel output data stream, ~~it~~ the first depuncturing element transmits to the second depuncturing element ~~(P1')~~ an indication signal ~~(data_valid)~~ which informs the second depuncturing element ~~(P1')~~ about empty locations in the parallel output data stream of the first depuncturing element ~~(P2')~~.

35. (Currently amended) The electronic receiver device as claimed in claim 34, ~~characterized in that~~ wherein the first depuncturing element ~~(P2') has~~comprises:

[[-]] a first multiplexer ~~(MUX)~~ having two inputs and one output,

[[-]] a second multiplexer ~~(MUX)~~ having two inputs and one output, and

[[-]] a third multiplexer ~~(MUX)~~ having four inputs and one output, in each case a 1-step delay register ~~(D)~~ is connected between

[[-]] the output of the first multiplexer ~~(MUX)~~ and one input of the second multiplexer ~~(MUX)~~,

[[-]] the output of the second multiplexer ~~(MUX)~~ and a first data output ~~(Out_X)~~ of the first depuncturing element ~~(P2')~~,

[[-]] the output of the third multiplexer ~~(MUX)~~ and a second data output ~~(Out_Y)~~ of the first depuncturing element ~~(P2')~~, and

[[-]] a first data input ~~(IN_Y)~~ of the first depuncturing element ~~(P2')~~ and an input of the third multiplexer ~~(MUX)~~, and

[[-]] the first data input ~~(IN_Y)~~ of the first depuncturing element ~~(P2')~~ is also directly electrically connected to an input of the first multiplexer ~~(MUX)~~ and to a further input of the third multiplexer ~~(MUX)~~,

[[-]] the second data input ~~(IN_X)~~ of the first depuncturing element ~~(P2')~~ is directly electrically connected to the further input of the second multiplexer ~~(MUX)~~, and the third input of the third multiplexer ~~(MUX)~~, and

[[-]] the respectively remaining input of the first multiplexer ~~(MUX)~~ and of the third multiplexer ~~(MUX)~~ is connected to a line on which soft zeros are made available.

36. (Currently amended) The electronic receiver device as claimed in claim 34 ~~or claim 35~~, ~~characterized in that~~ wherein the second depuncturing element ~~(P1') has~~ comprises three multiplexers ~~(MUX)~~ each with two inputs and one output, in each case a 1-step delay register ~~(D)~~ is connected between

[[-]] the output of the first multiplexer ~~(MUX)~~ and an input of the second multiplexer ~~(MUX)~~,

[[-]] the output of the second multiplexer ~~(MUX)~~ and the first data output ~~(Out_X)~~ of the second depuncturing element ~~(P1')~~, and

[[-]] the output of the third multiplexer ~~(MUX)~~ and the second data output ~~(Out_Y)~~ of the second depuncturing element ~~(P1')~~, and

[[-]] the first data input ~~(IN_X)~~ of the second depuncturing element ~~(P1')~~ is directly electrically connected to an input of the first multiplexer ~~(MUX)~~ and to the further input of the second multiplexer ~~(MUX)~~,

[[-]] the second data input ~~(IN_Y)~~ of the second depuncturing element ~~(P1')~~ is directly electrically connected to an input of the third multiplexer ~~(MUX)~~, and

[[-]] the respectively remaining input of the first multiplexer and of the third multiplexer ~~(MUX)~~ is connected to a line on which soft zeros are made available.

37. (Currently amended) The electronic receiver device as claimed in ~~one of~~ claim[[s]] 34 ~~to 36~~, ~~characterized in that~~wherein:

[[-]] the first depuncturing element ~~(P2') has~~ comprises a first and a second data output and is configured in such a way that ~~it~~ the first depuncturing element distributes its output data stream ~~essentially~~ substantially uniformly between its two data outputs, and

[[-]] the second depuncturing element ~~(P1') has~~ comprises a first and a second data input, the first data input of the second depuncturing element ~~(P1')~~ being directly or indirectly electrically connected to the first data output of the first depuncturing element ~~(P2')~~, and the second data input of the second depuncturing element ~~(P1')~~ is directly or

indirectly electrically connected to the first data output of the first depuncturing element ~~(P2')~~.

38. (Currently amended) The electronic receiver device as claimed in ~~one of~~ claim[[s]] 34 ~~to 37~~, ~~characterized in that~~wherein
[[-]] the second depuncturing element ~~(P1')~~ is configured in such a way that, using the ~~said~~ indication signal ~~(data_valid)~~ which is additionally transmitted by the first depuncturing element ~~(P2')~~, ~~it~~ the second depuncturing element detects the empty locations in the parallel input data stream coming from the first depuncturing element ~~(P2')~~ and fills them with soft zeros during the further data processing.

39. (Currently amended) The electronic receiver device as claimed in ~~one of~~ claim[[s]] 34 ~~to 38~~, ~~characterized in that~~ wherein the first depuncturing element ~~(P2')~~ ~~has~~ comprises two data inputs.

40. (Currently amended) The electronic receiver device as claimed in claim 39, ~~characterized in that~~ wherein the two data inputs of the first depuncturing element ~~(P2')~~ are simultaneously the two data inputs of the depuncturing device.

41-45. (Canceled).